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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/769,534	01/26/01	AKIYOSHI H	108397-00025

EXAMINER	
ENGLUND, T	
ART UNIT	**PAPER NUMBER**
2816	

MM41/1107
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/769,534	Applicant(s) AKIYOSHI, HIDEO	
	Examiner Terry L Englund	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to because "(PROL)" of fig. 2 should be --(PORL)-- to ensure the signal label corresponds to the other figures and their descriptions. Correction is required.

Specification

The title of the invention is rather general and can also be considered misleading. For example, although the applicant's Fig. 1 can be considered an integrated circuit, it is believed it initializes an integrated circuit (cited as "an internal circuit" within the claims), which is not shown, with the signal POR. Therefore, since the title appears to imply the "integrated circuit" to be initialized is the main part of the application, a new title is required that is clearly indicative of the invention to which the claims are directed. It is suggested the title be changed to --POR circuit/method with wide, operational margin-- or --Power-on Reset circuit/method for initializing an integrated circuit--.

The disclosure is objected to because of the following informalities: It is not clear what is meant by "channel length...is shorted" on page 1, lines 25-26. Was --shorter-- meant? Page 4, line 27 "second" should be --third-- since Fig. 4 shows the second embodiment already, and page 9 (line 17) identifies Fig. 5 as the "third embodiment."

Page 9, lines 32 and 35 should have --38-- instead of "36." Appropriate corrections are required.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 4, and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. In each of claims 2, 4 and 6, the phrase "for each of said sub power-on reset" is inaccurate and/or misleading. The phrase appears to imply each of the pulse generators generates its respective pulse in response to each of the reset signals (e.g. sub power-on or external power-on). However, as shown in the applicant's own figures, each pulse generator generates its own pulse in synch with a respective one of the reset signals, not each of them.

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Malherbe. In Fig. 3, Malherbe shows an integrated circuit comprising a sub reset signal generator CE1-CEn for generating a plurality of sub power-on reset signals POR1-

PORn; and a main reset signal generator OR for generating a main power-on reset signal POR to initialize an internal circuit (related to the disclosed "an inhibiting means (not shown) placed downline from the control circuit CC" on lines 7-10 on column 5) in response to (at least one of) the reset signals POR1-PORn. Fig. 4 shows details of each sub reset signal generator CE1-CEn. Since each generator has a different configuration, their respective reset signal will have a different timing than the others, anticipating claim 1. Fig. 3 also shows a reset terminal (unlabeled) for receiving an external power-on reset signal TPOR, thus anticipating claims 3 and 5. Referring to Fig. 4, and interpreting the circuit differently, the sub reset signal generator is deemed the elements10,11,21,20,30-32 which generates a plurality of sub power-on reset signals (e.g. the outputs of 10/11; 21/20; and 30/31/32) at different timings (due to the different configurations of the elements). The main reset signal generator comprises elements 12-16,22-24,33-36,OR for generating a main power-on reset signal POR in response to the sub power-on reset signals, thus anticipating claim 1 also. Since the main reset signal generator comprises a plurality of pulse generators (i.e. 12-16, 22-24, and 33-36) and a composite circuit OR for generating the main power-on reset signal POR, claim 2 is anticipated. [It is noted each pulse generator will generate a pulse in synch with a transition edge of a respective sub power-on reset signal. For example, when the rising edge of the voltage (sub power-on reset signal) between elements 10 and 11 reaches the switching threshold of inverter 12,13, generator 12-16 will provide an associated transition pulse.] Using the same type of reasoning as applied above, elements 50,51 of Fig. 5 are deemed a means for providing an external power-on reset signal to a reset

terminal - (of comparator 52), and comparator 52 is deemed one of the plurality of pulse generators. Therefore, composite circuit OR generates the main power-on reset signal in response to the sub power-on reset signal(s) and external power-on reset signal, anticipating claims 4 and 6. When considering Figs. 3-5, one of ordinary skill in the art would recognize 12-16, 22-24, 33-36, and 52 generate a plurality of power-on reset signals (i.e. POR1, POR2, PORn, and TPOR, respectively) according to a plurality of sub power-on reset signals (from 10/11, 20/21, 30/31/32, and 50/51, respectively), and OR initializes an internal circuit (not shown) by signal POR according to (at least one of) the power-on reset signals. Therefore, claim 7 is also anticipated.

Claims 1-3, 5, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Crotty also. Crotty shows a circuit in Fig. 6 with blocks 630,640,650,210,220 closely corresponding to blocks 10,16,20,12,18, respectively of the applicant's own Fig. 1. Fig. 6 shows a sub reset signal generator 630,210 for generating a plurality of sub power-on reset signals VD2,VD1; and a main reset signal generator 640,220,650 for generating a main power-on reset signal POR according to at least one of the sub power-on reset signals. Signal POR is used to initialize an internal circuit (not shown but disclosed as logic circuits or IC devices (e.g. see column 1, lines 6-31)). Since the configurations of circuits 630 and 210 are different from each other (e.g. see details of 630 in Fig. 8(a), and of 210 in Figs. 3(a) and 3(d)), their respective reset signals VD2 and VD1 will have different timings from each other, thus anticipating claim 1. The main reset signal generator 640,220,650 comprises a plurality of pulse generators 640,220 and a composite circuit 650. Each pulse generator 640,220 of Crotty could be configured as

shown in Fig. 4(a), with details of the delay circuit 420 shown in Fig. 5(a). Deeming inverters 512-516 of Fig. 5(a) a delay in series with inverter 518, each pulse generator of Crotty would then correspond to the pulse generators 16,18 shown in the applicant's own Fig. 1, wherein each generator comprises a delay 22, inverter 24, and NAND gate 26. Fig. 7 of Crotty shows details of block 650. It comprises a NAND gate and inverter coupled in series, wherein the NAND gate receives the POR1,POR2 signals and generates signal POR. Therefore, claim 2 is also anticipated. Blocks 640,220 generate a plurality of power-on reset signals POR2,POR1 according to a plurality of sub power-on reset signals VD2,VD1, and block 650 initializes an internal circuit (not shown) according to at least one of the power-on reset signals POR2,POR1, anticipating claim 7. Fig. 10 of Crotty shows another embodiment of the circuit. This embodiment comprises a sub reset signal generator 630,210,930 for generating sub power-on reset signals POR2,POR1; a reset terminal (not labeled) for receiving an external power-on reset signal POR3; and a main reset signal generator 1010 for generating a main power-on reset signal POR. Therefore, applying the same type of reasoning as previously described (with respect to different timings, and the initialization of an internal circuit according to at least one reset signal), claims 3 and 5 are also anticipated.

No claim is allowable.

Although not used for any formal rejections described above, the other prior art references cited on the accompanying PTO-892 are deemed relevant to at least some of the broad independent claims. For example, Fig. 5 of Shin clearly shows a circuit generating a plurality of what could be deemed sub power-on reset signals with different

timings (e.g. see OUT_A,OUT_B of Figs. 6C,6G; or A2,B2,N2 of Figs. 6E,6H,GI), and a main reset signal generator (e.g. see 8,9) for generating a main power-on reset signal OSCEN2. Also note that Fig. 5 shows what can be deemed a reset terminal for receiving an external power-on reset signal PWROKB. Lee (e.g. Fig. 2) is another example that shows a circuit comprising sub reset signal generator 140,150 for providing a plurality of sub power-on reset signals NR20,NR30; a reset terminal 180; and a main reset signal generator ND1,160,170 for providing what can be deemed a main power-on reset signal NR41. Therefore, these references should be carefully reviewed and considered.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for this Art Unit is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund

2 November 2001

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